



Fig. 1 PRIOR ART

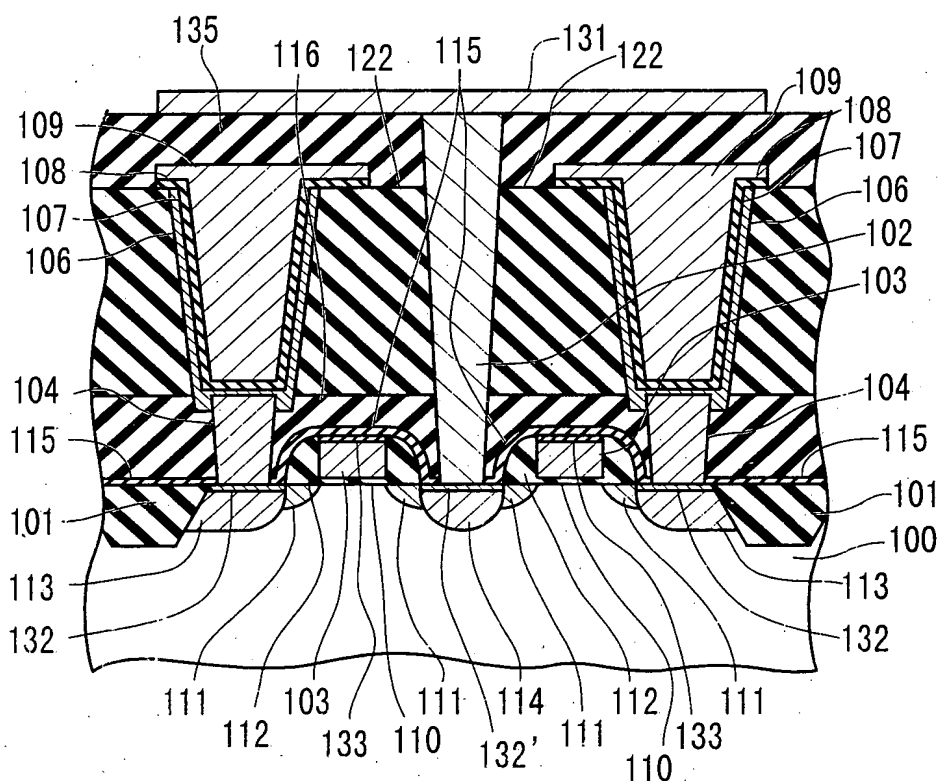
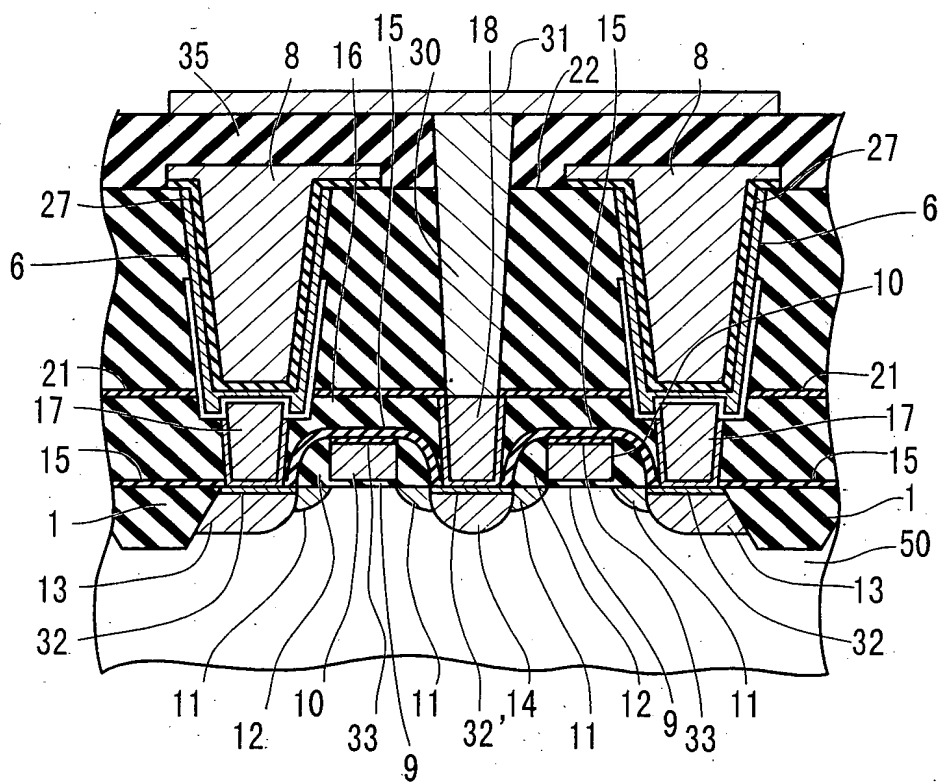
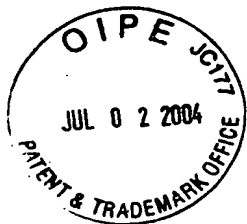




Fig. 2





F i g . 3

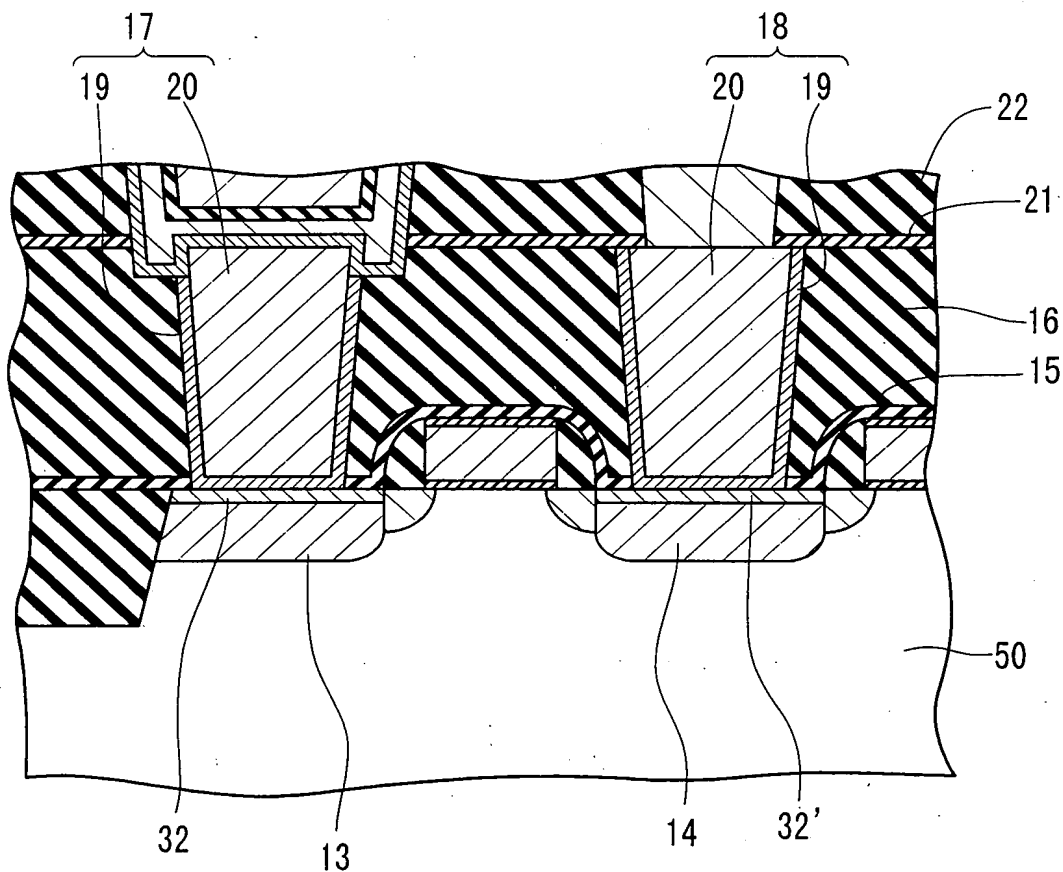
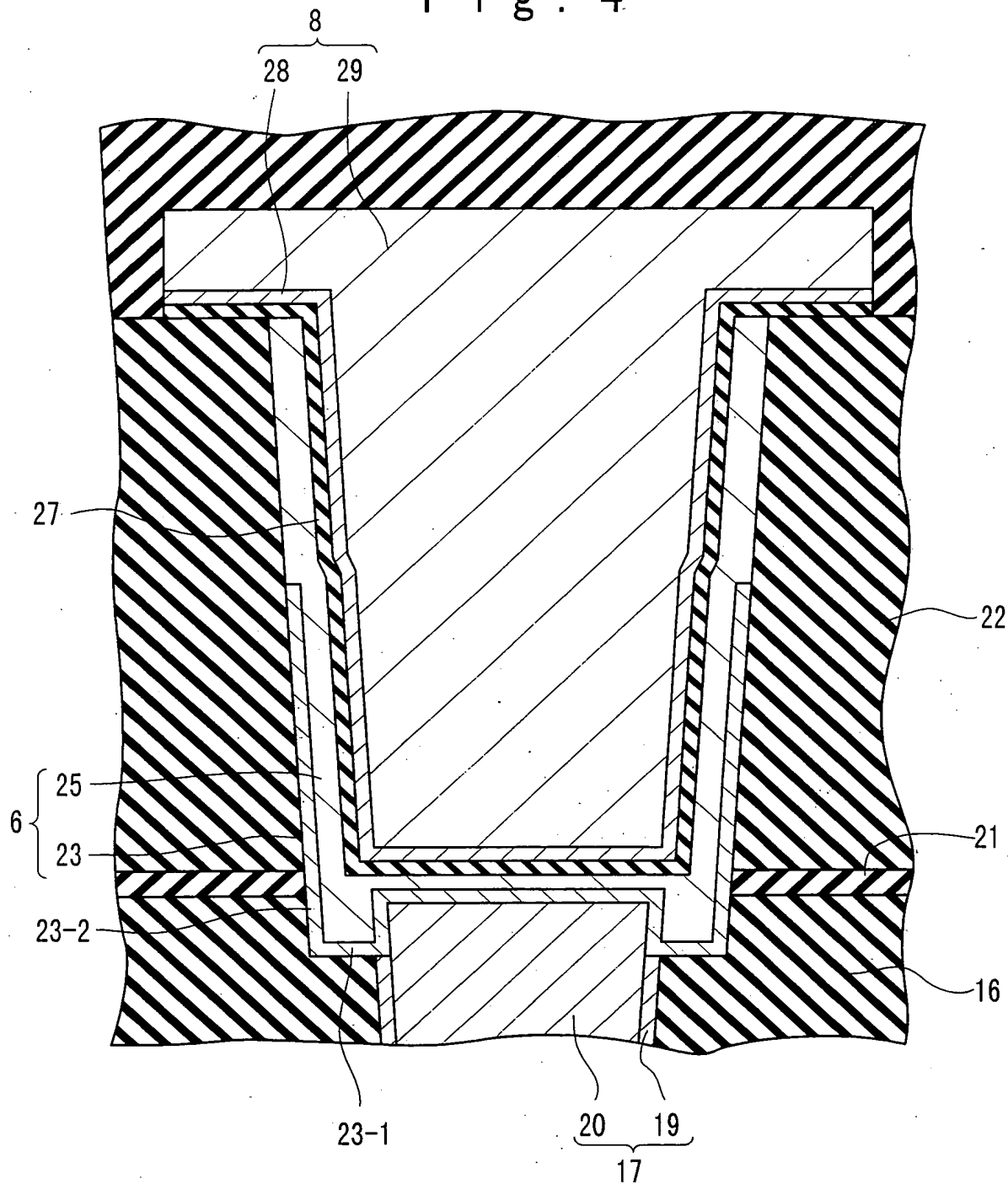




Fig. 4





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Fig. 5

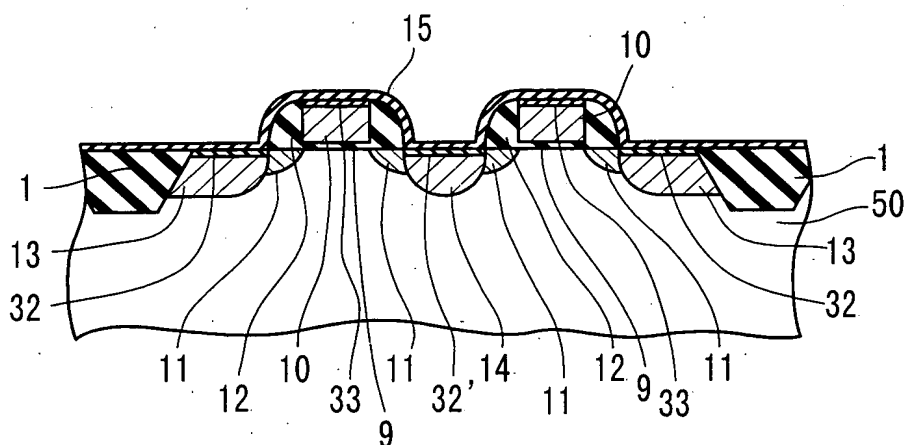
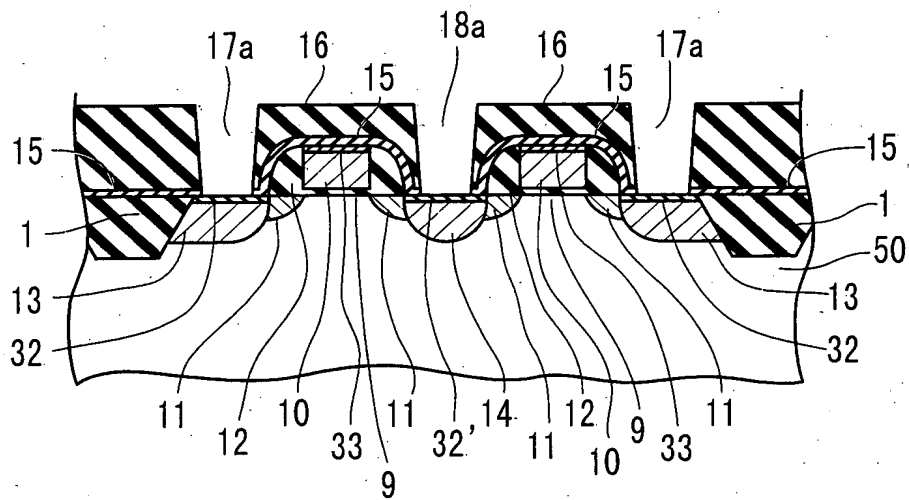




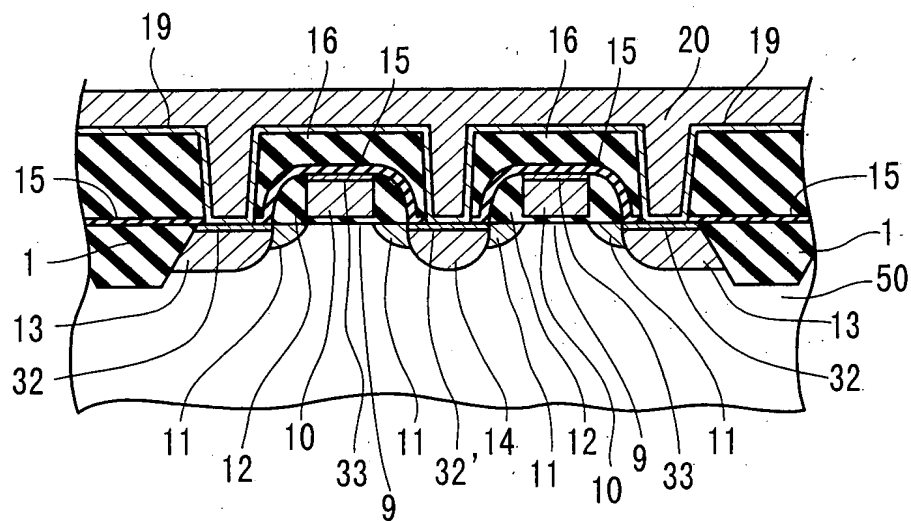
Fig. 6





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APPLN No.: 10/068,893
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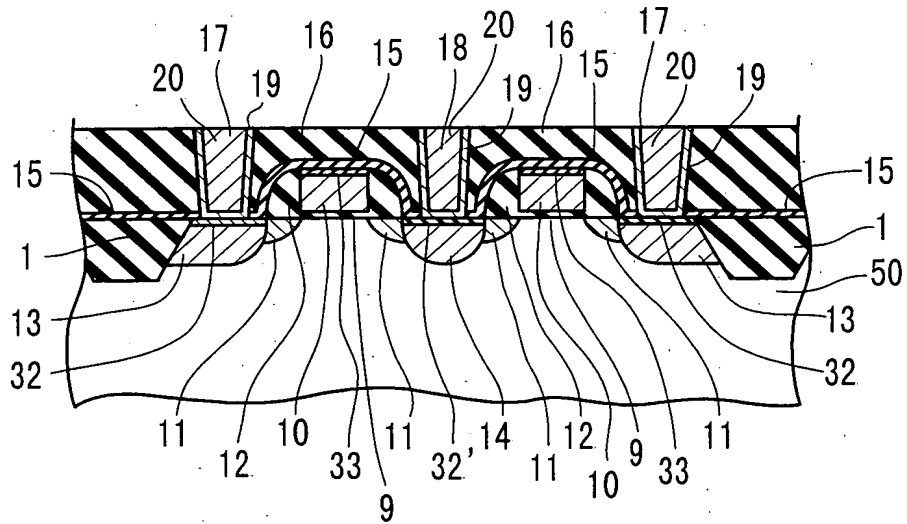
Fig. 7





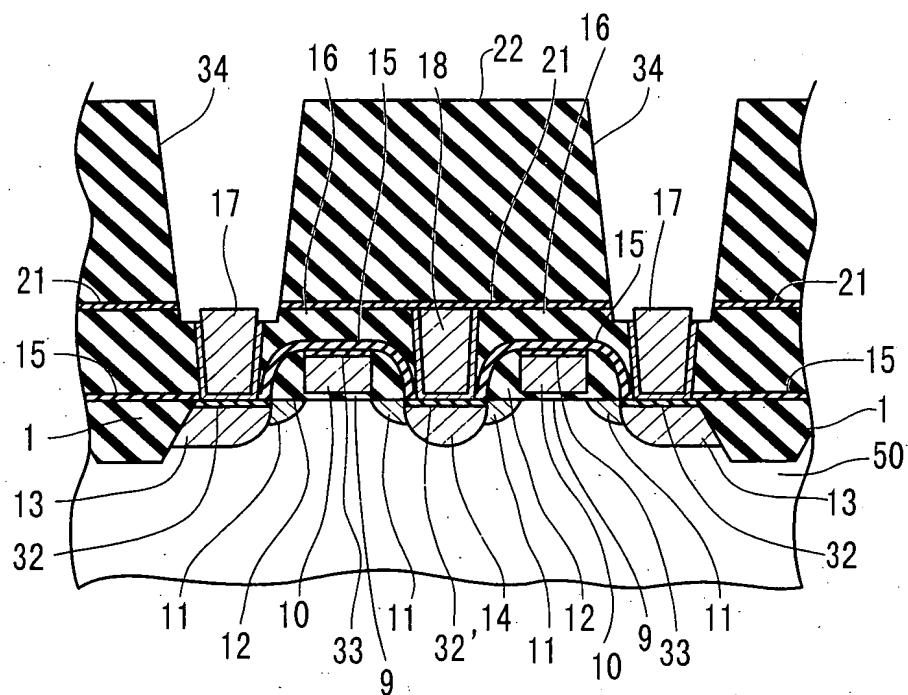
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REPLY TO NOTICE OF ALLOWABILITY OF: MAY 25, 2004
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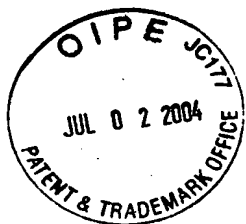
F i g . 8





F i g . 9





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Fig. 10

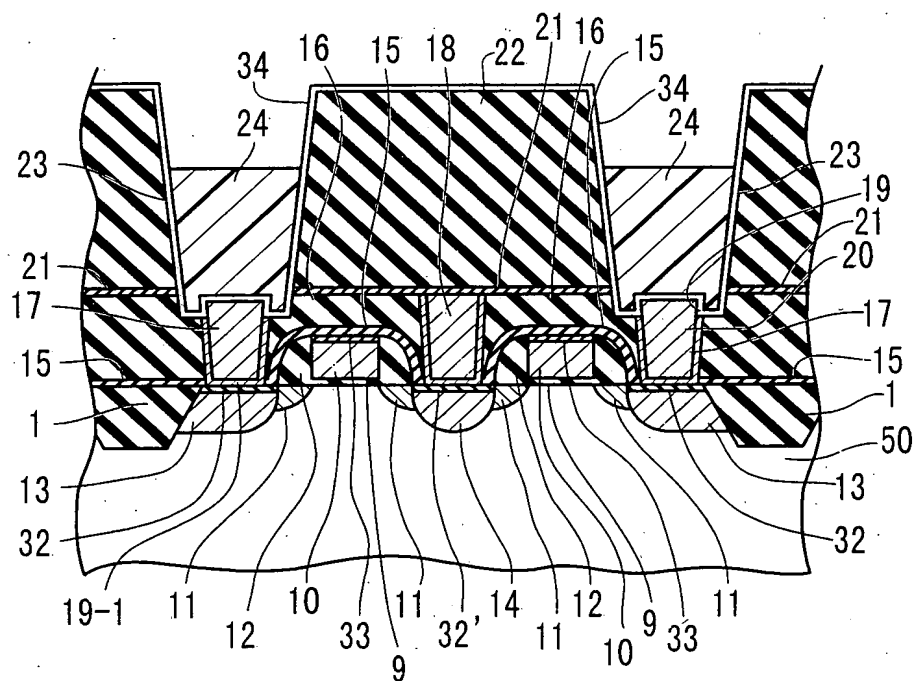
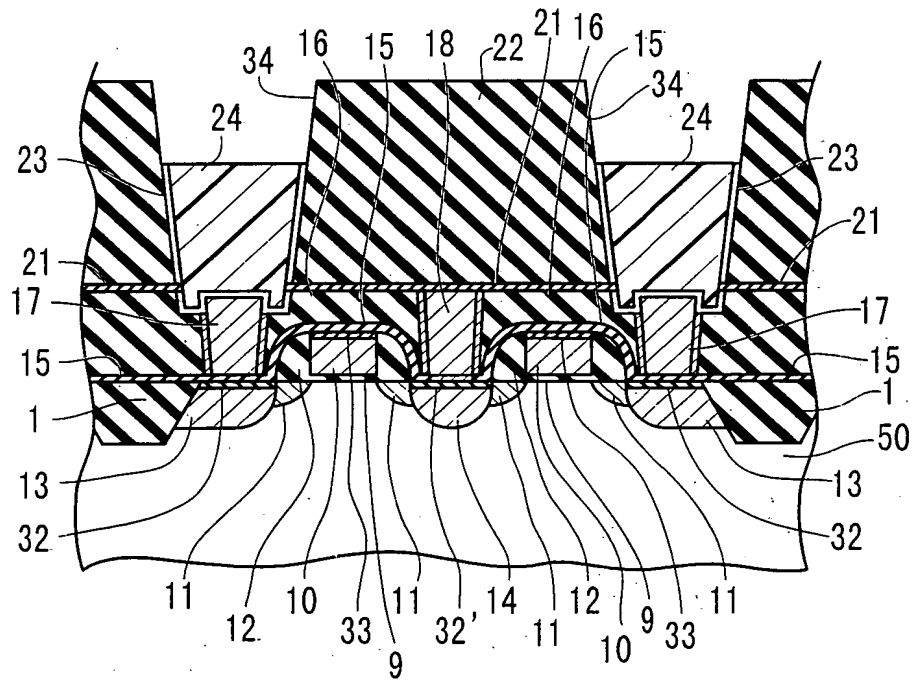




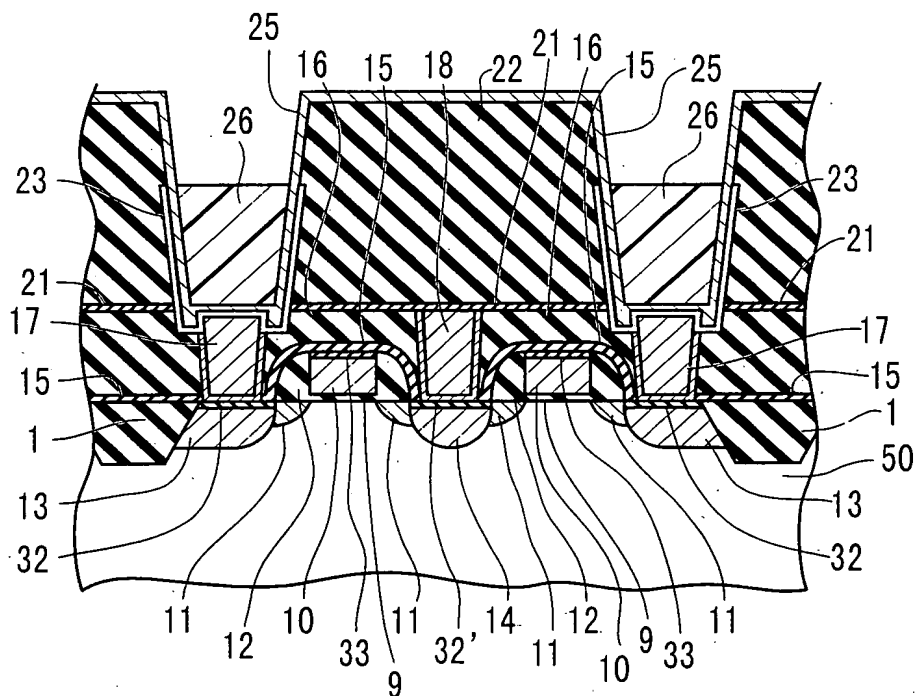
Fig. 11





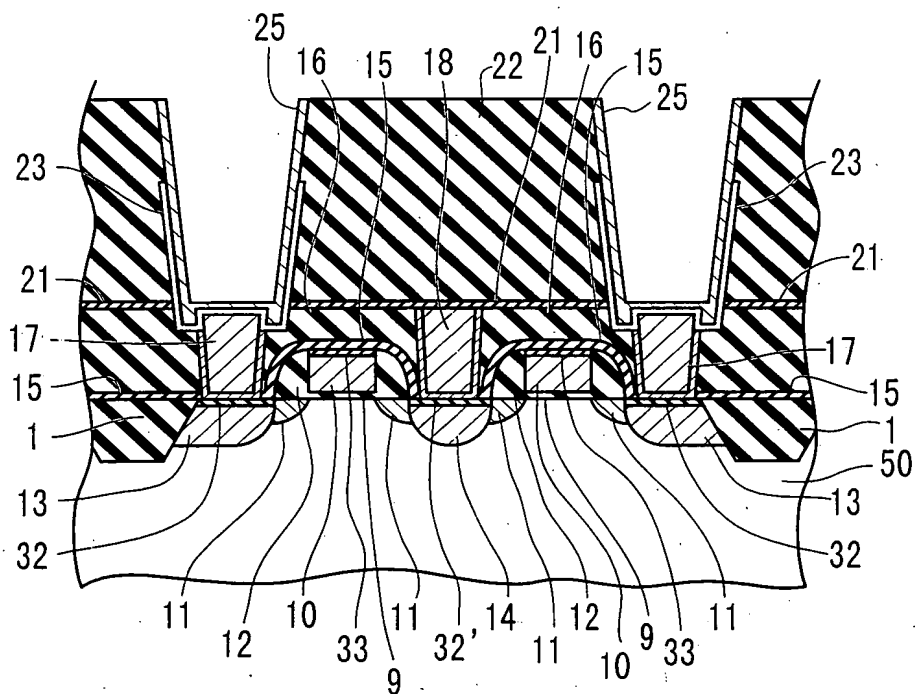
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REPLACEMENT SHEET

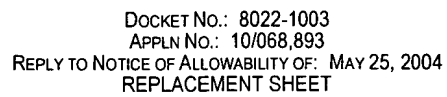
Fig. 12





F i g . 1 3





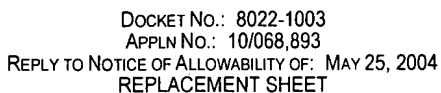


Fig. 16

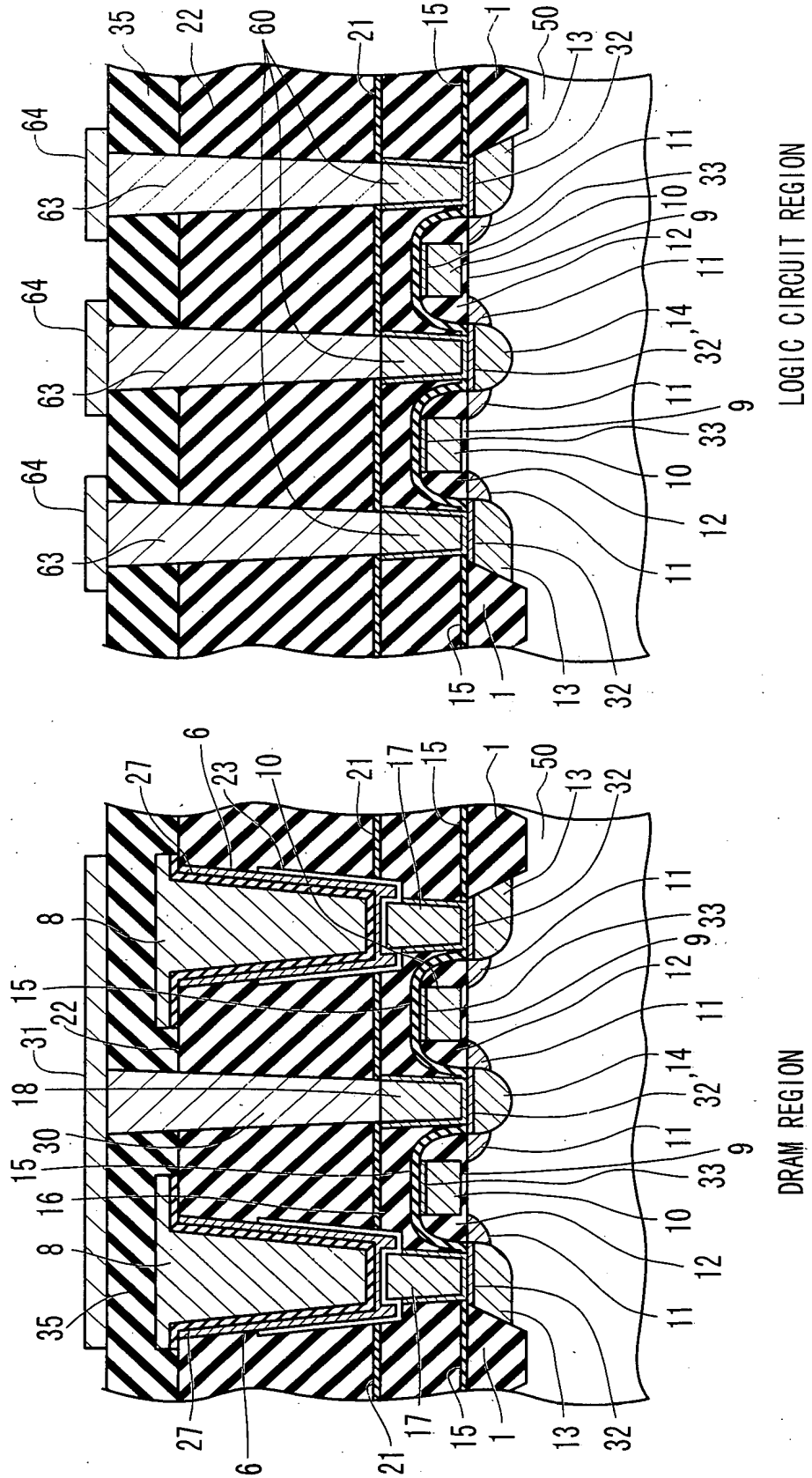
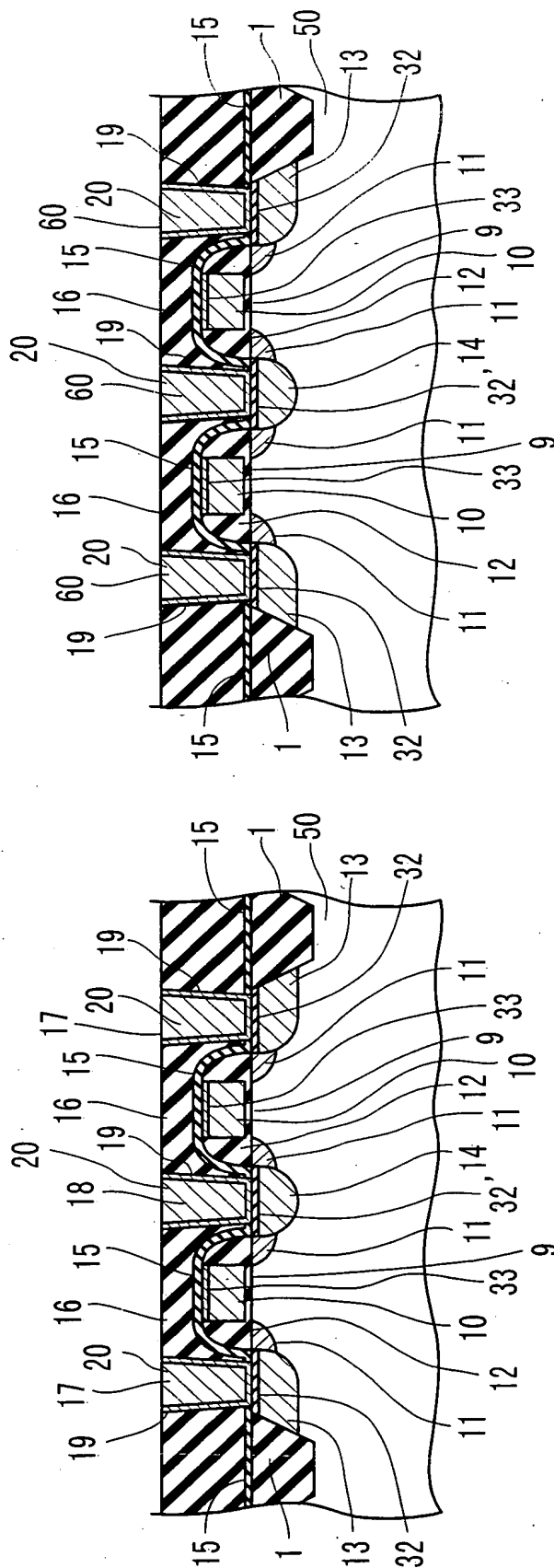




Fig. 17



DRAM REGION

LOGIC CIRCUIT REGION

Fig. 18

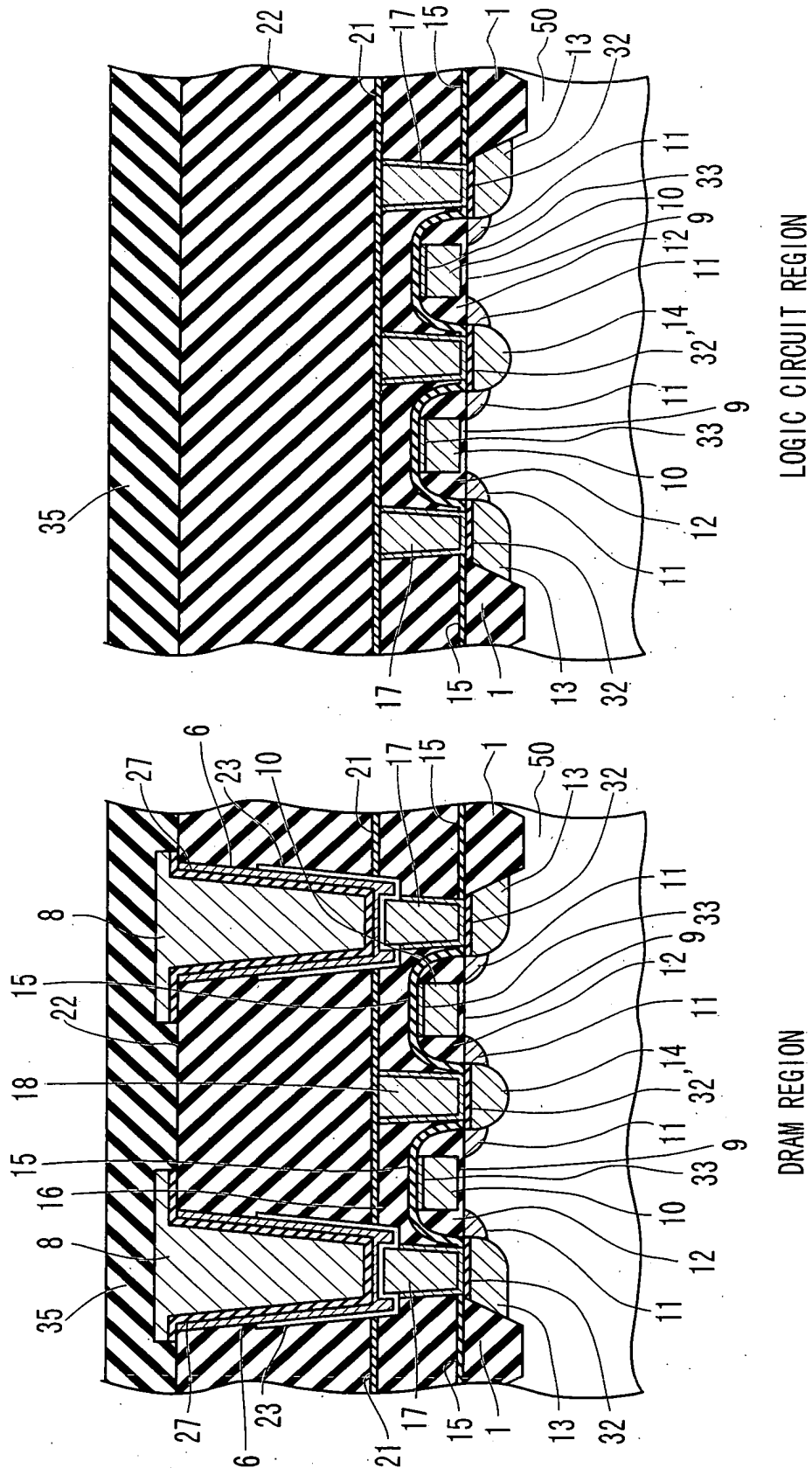




Fig. 19

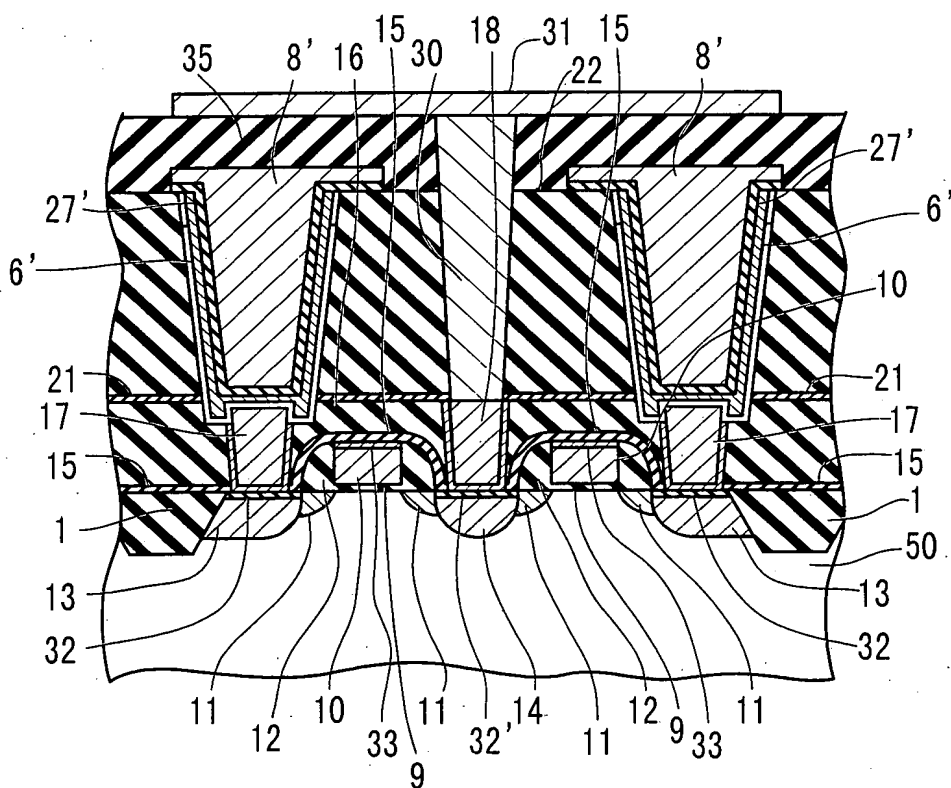
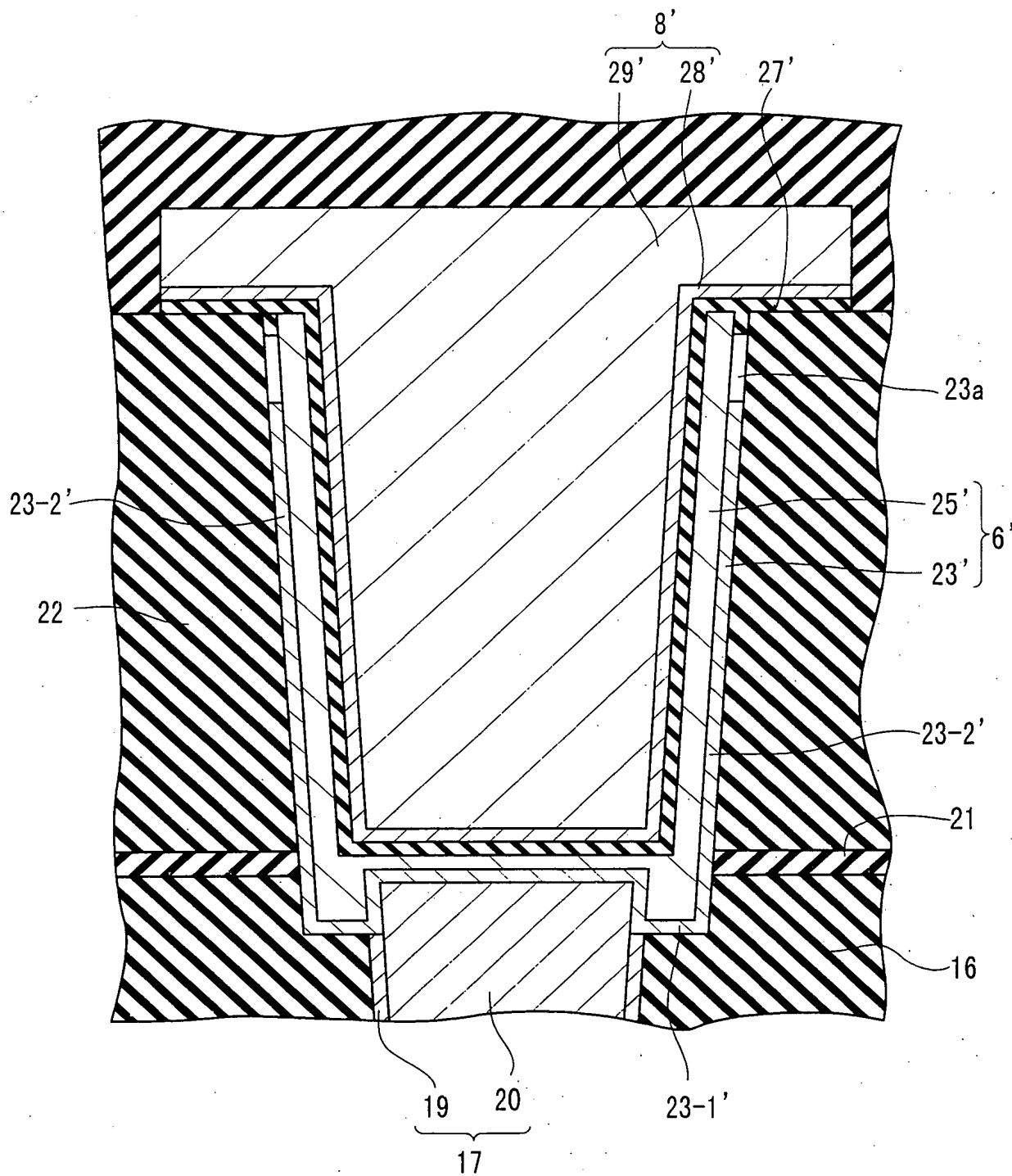


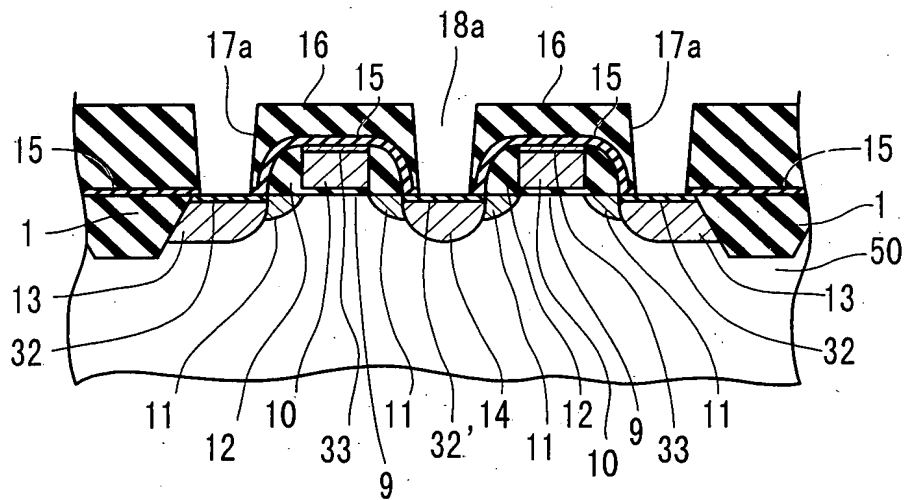


Fig. 20



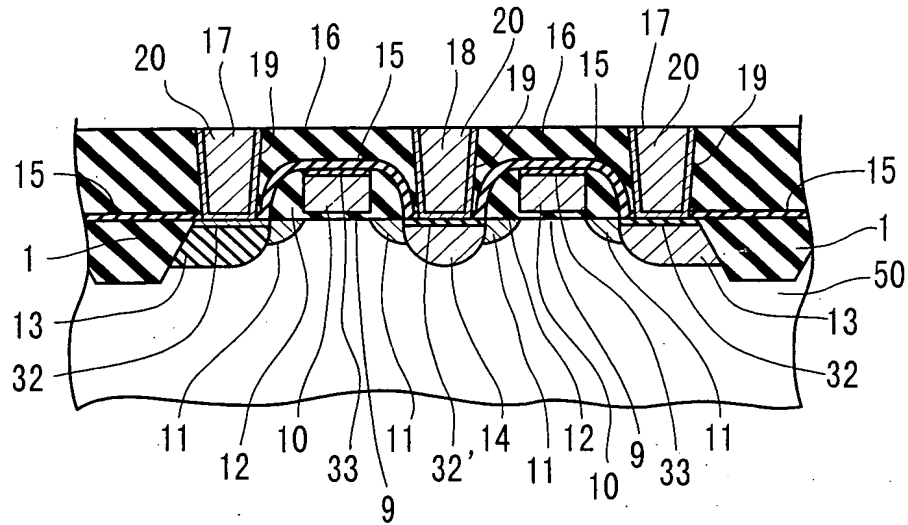


F i g . 2 1





F i g . 2 2



F i g . 2 3

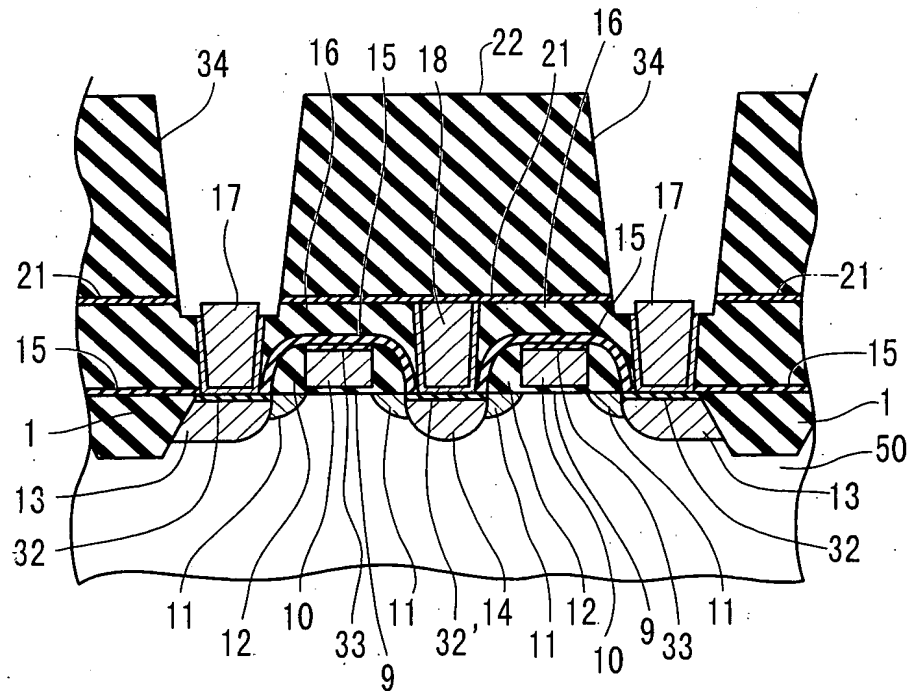
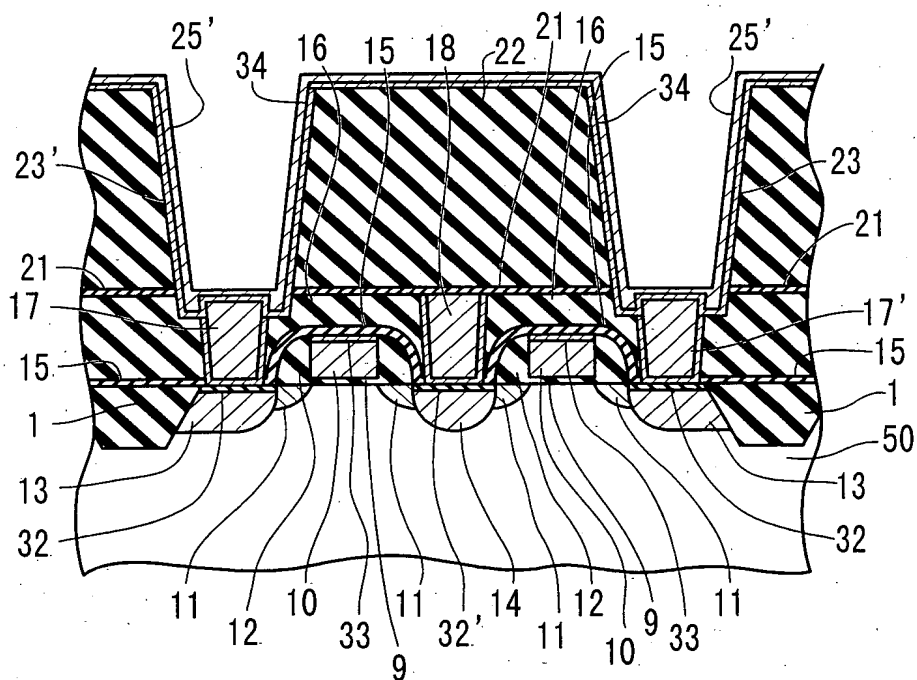




Fig. 24



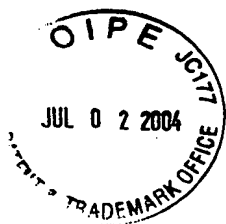


Fig. 25

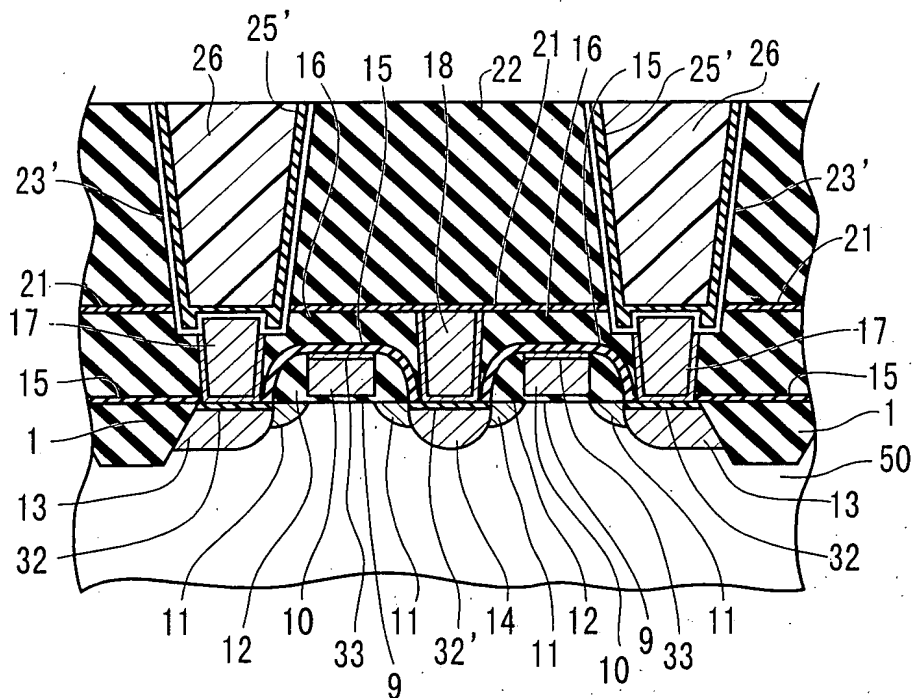


Fig. 26

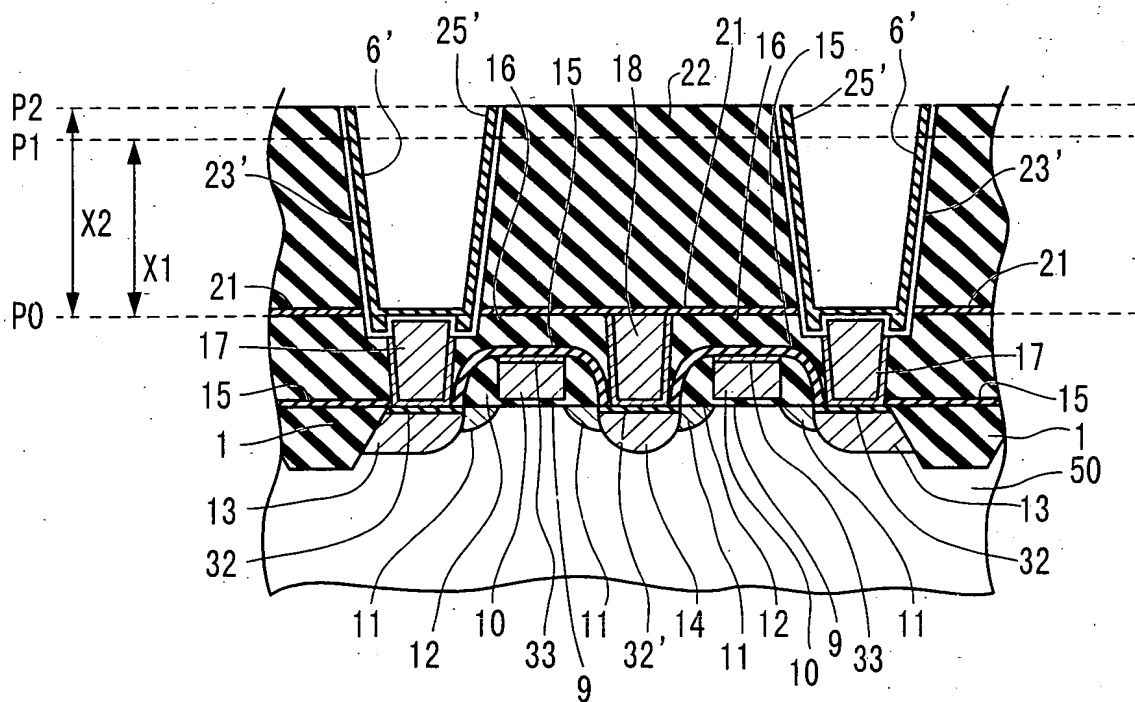
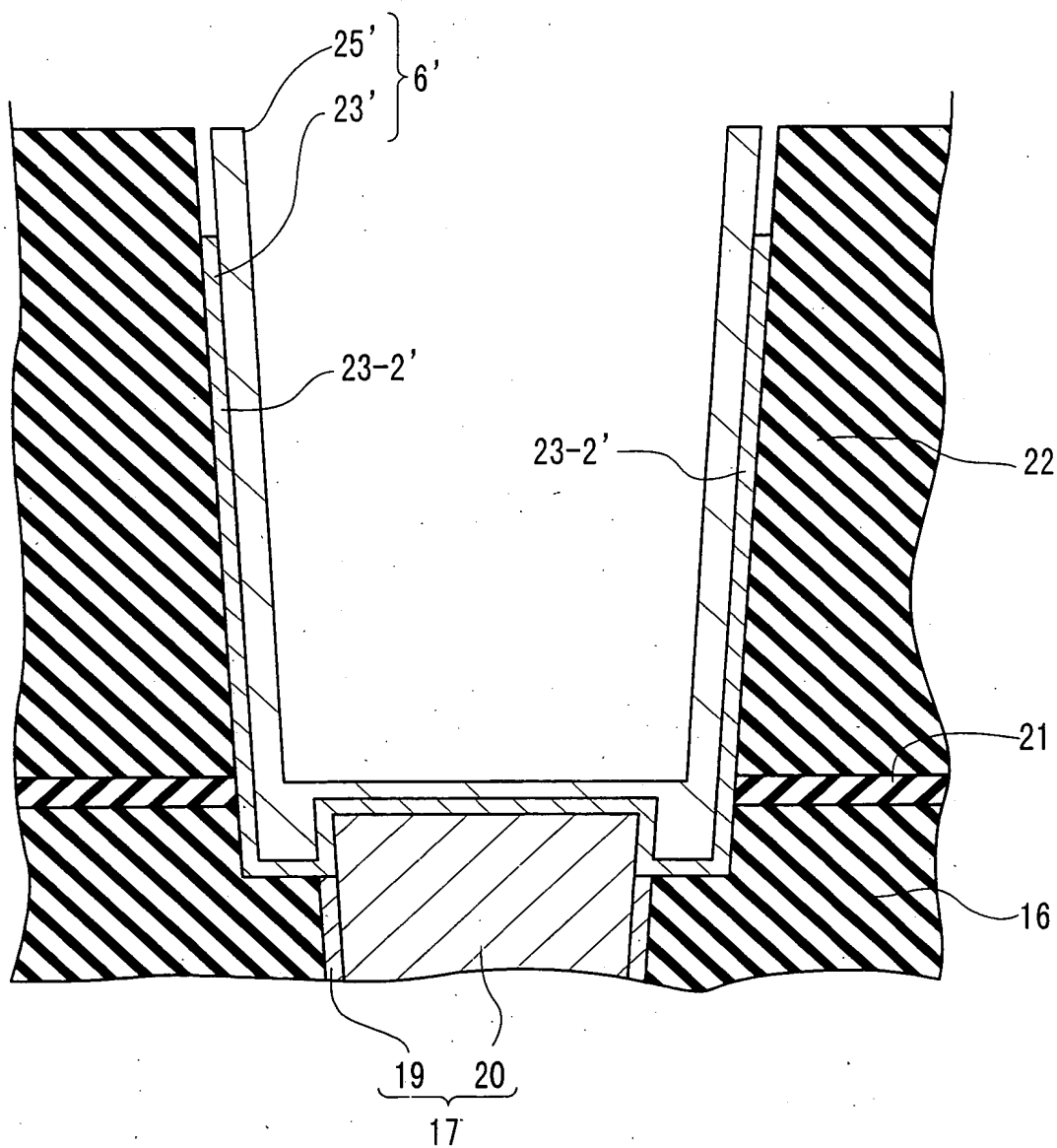


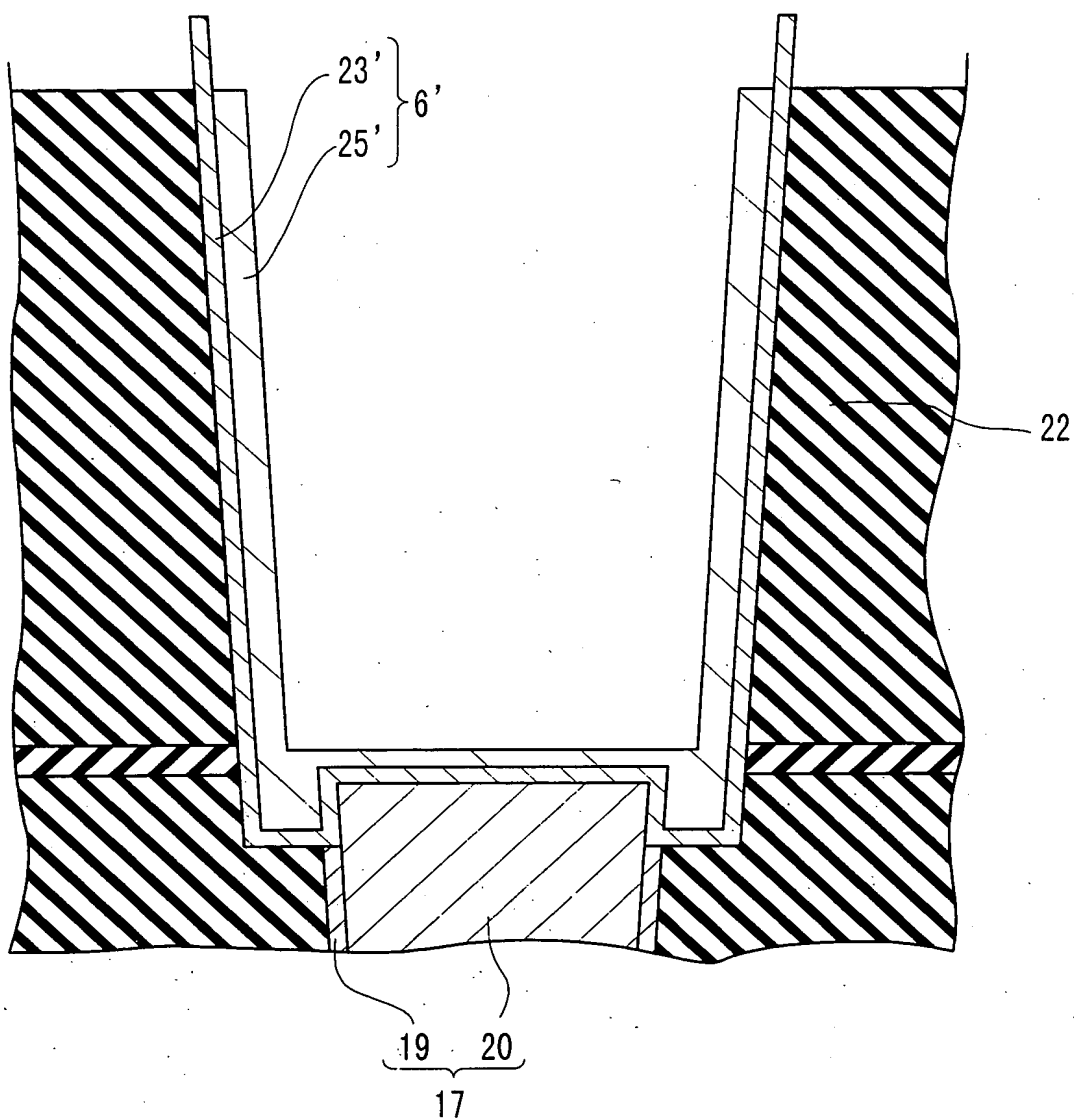


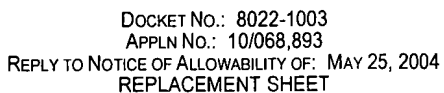
Fig. 27





F i g . 2 8







F i g . 3 0

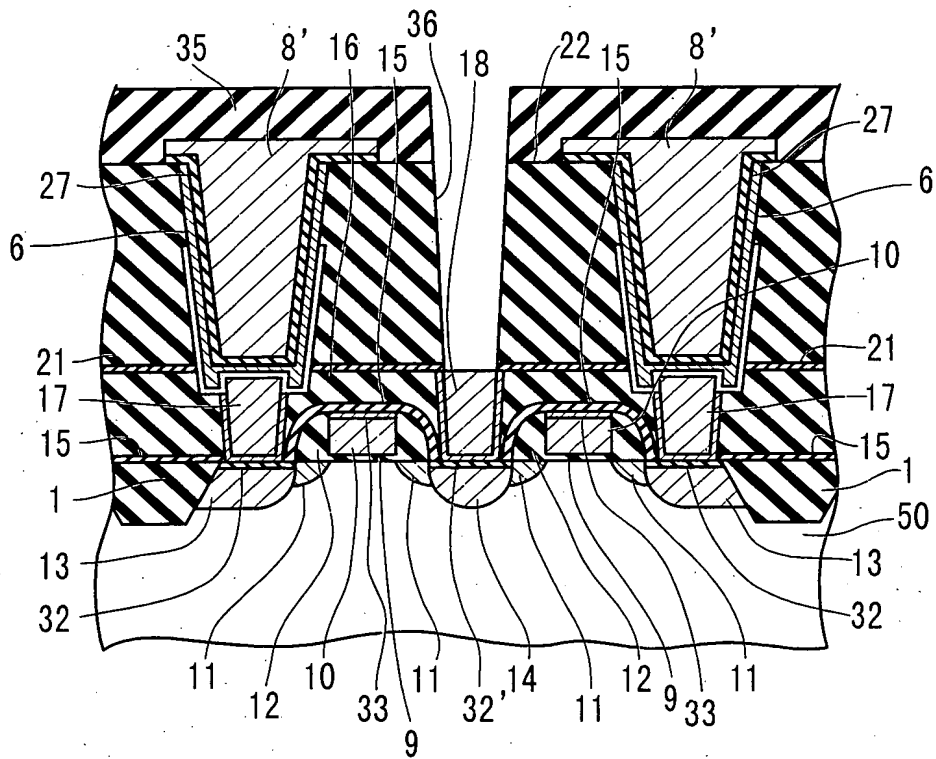




Fig. 31

